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Abstract
With lossless compression, the raw or original source data is recovered exactly after decompression is bring employed as a means that can bring significant advantages to computing systems. In recent years, due to the combination of pressure for more bandwidth allied and the need to improve storage capacity, the successful applications of lossless data compression have been increasing in the fields of storage systems, data transmission systems and communication networks. However, in systems that operate at a data rate of over Gbits/s, the data compression is not used to its full benefits subjected to performance limitations encountered in the data compression hardware.
In this thesis, we presented an improved algorithm and its hardware architecture of a high-speed lossless compressor that utilizes the CAM-based dictionary where multiple symbols are processed per cycle to provide the specified performance to improve the efficiency of data compression at a gigabit per second bandwidth. Further, the proposed hardware implementation with low complexity, low cost and 1.6 Gbits/s high data throughputs has been verified via the Altera APEX20KE EP20K200EFC484-1 FPGA technology. The simulation result shows that the clock rate of the proposed high-speed lossless compressor can to be 50MHz and the compression ratio (Input/Output) approximated to 0.55.
Moreover, considering the ASIC implementation, the aforementioned Gbits/s lossless data compression architecture has been synthesized with the TSMC 0.35μm cell library. The size of the resulting circuit is about 21572 gate counts and the chip area is evaluated to be 3044μm×2993.7μm. In the meanwhile, the clock speed can come to 100MHz. Therefore, we can see that the design and implementation of the proposed lossless compressor can effectively achieve better data compression throughputs and compression ratio in a system operating at a Gbits/s bandwidth.
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